

Multi-layer Grid Embeddings

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Abstract

In this paper we propose two new multi-layer grid models for VLSI layout, both of which take into account the number of contact cuts used. For the first model in which nodes “exist” only on one layer, we prove a tight area \times (number of contact cuts) = $\Theta(n^2)$ trade-off for embedding any degree 4 n -node planar graph in two layers. For the second model in which nodes “exist” simultaneously on all layers, we prove a number of bounds on the area needed to embed graphs using no contact cuts. For example we prove that any n -node graph which is the union of two planar subgraphs can be embedded on two layers in $O(n^2)$ area without contact cuts. This bound is tight even if more layers and an unbounded number of contact cuts are allowed. We also show that planar graphs of bounded degree can be embedded on two layers in $O(n^{1.6})$ area without contact cuts.

These results use some interesting new results on embedding graphs in a single layer. In particular we give an $O(n^2)$ area embedding of planar graphs such that each edge makes a constant number of turns, and each exterior vertex has a path to the perimeter of the grid making a constant number of turns. We also prove a tight $\Omega(n^3)$ lower bound on the area of grid n -permutation networks.